TMUX1208-Q1 5-V Bidirectional 8:1 Multiplexer with 1.8-V Logic

1 Features

- AEC-Q100 Qualified for Automotive Applications
  – Temperature Grade 1: –40°C to 125°C, T_A
- Low On-resistance: 5 Ω
- Wide Supply Range: 1.08 V to 5.5 V
- Rail to Rail Operation
- Bidirectional Signal Path
- 1.8 V Logic Compatible
- Fail-Safe Logic
- Low Supply Current: 10 nA
- Transition Time: 14 ns
- Break-before-make Switching
- ESD Protection HBM: 2000 V
- Small QFN Package

2 Applications

- Analog and Digital Multiplexing / Demultiplexing
- Automotive Head Unit
- Telematics Control Unit
- Emergency Call (eCall)
- Infotainment
- Body Control Modules (BCM)
- Body Electronics and Lighting
- Battery Management Systems (BMS)
- HVAC Controller Module
- ADAS Domain Controller

3 Description

The TMUX1208-Q1 is a general purpose complementary metal-oxide semiconductor (CMOS) multiplexer (MUX). The TMUX1208-Q1 is an 8:1 mux configuration allowing 8 different signal paths to be switched to a common output pin . Wide operating supply of 1.08 V to 5.5 V allows for use in automotive applications with varying power supply requirements. The device supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from GND to V_{DD}.

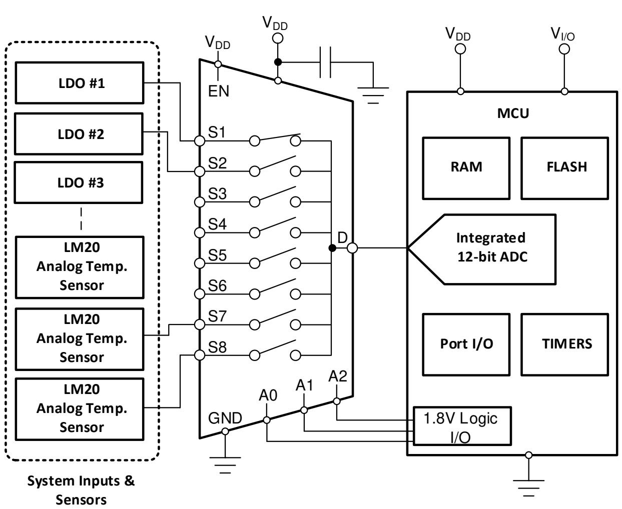
The TMUX1208-Q1 comes in a small QFN package to enable reduced system size requirements. The device has low on-resistance of 5Ω typical to minimize the impact of distortion and signal integrity issues when the device is not connected to a high impedance signal path.

All logic inputs have 1.8 V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

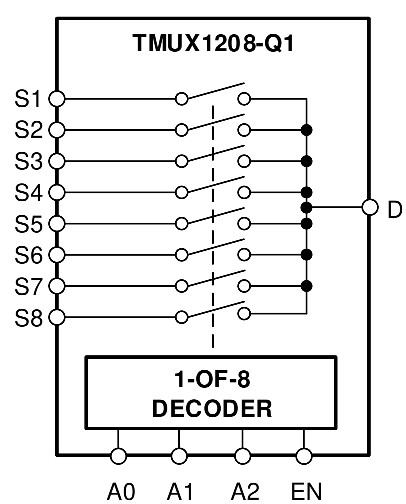
Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TMUX1208-Q1	QFN (16)	2.60 mm x 1.80 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Application Example



TMUX1208-Q1 Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August, 2019) to Revision A (July, 2020)	Page
• Releasing data sheet as production data	1

5 Pin Configuration and Functions

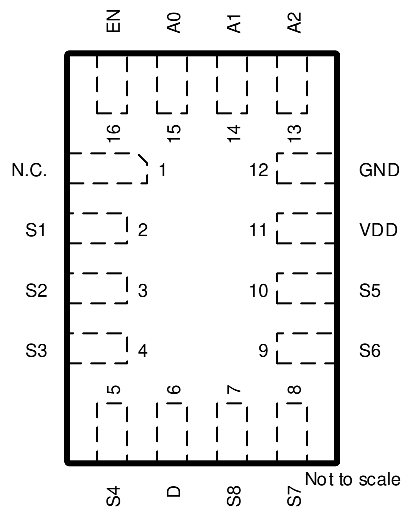


Figure 5-1. RSV Package 16-Pin QFN Top View

Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	UQFN		
A0	15	I	Address line 0. Controls the switch configuration as shown in Table 8-1.
EN	16	I	Active high logic input. When this pin is low, all switches are turned off. When this pin is high, the A[2:0] address inputs determine which switch is turned on.
N.C.	1	Not Connected	Not Connected
S1	2	I/O	Source pin 1. Can be an input or output.
S2	3	I/O	Source pin 2. Can be an input or output.
S3	4	I/O	Source pin 3. Can be an input or output.
S4	5	I/O	Source pin 4. Can be an input or output.
D	6	I/O	Drain pin. Can be an input or output.
S8	7	I/O	Source pin 8. Can be an input or output.
S7	8	I/O	Source pin 7. Can be an input or output.
S6	9	I/O	Source pin 6. Can be an input or output.
S5	10	I/O	Source pin 5. Can be an input or output.
VDD	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	12	P	Ground (0 V) reference
A2	13	I	Address line 2. Controls the switch configuration as shown in Table 8-1.
A1	14	I	Address line 1. Controls the switch configuration as shown in Table 8-1.

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2] [3]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	6	V
V_{LOGIC}	Logic control input pin voltage (EN, A0, A1, A2)	–0.3	6	V
I_{LOGIC}	Logic control input pin current (EN, A0, A1, A2)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–30	30	mA
I_{IK}	Diode clamp current[4]	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Signal path pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{LOGIC}	Logic control input pin voltage (EN, A0, A1, A2)	0		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TMUX1208-Q1 RSV (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (VDD = 5 V ±10 %)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		5		Ω
			–40°C to +85°C			7	Ω
			–40°C to +125°C			9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		0.15		Ω
			–40°C to +85°C			1	Ω
			–40°C to +125°C			1	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		1.5		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		3		Ω
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1 V V_S = 1 V / 4.5 V Refer to Figure 7-2	25°C		±75		nA
			–40°C to +85°C	-150		150	nA
			–40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1 V V_S = 1 V / 4.5 V Refer to Figure 7-2	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1 V Refer to Figure 7-3	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Input logic high		-40°C to 125°C	1.49		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.10	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.02		µA
			–40°C to +125°C			2.7	µA

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-4	25°C		14		ns
			–40°C to +85°C			33	ns
			–40°C to +125°C			33	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-5	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			20	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		11		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			20	ns
Q_C	Charge Injection	$V_S = V_{DD}/2$ R_S = 0 Ω, C_L = 1 nF Refer to Figure 7-7	25°C		-8		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-8	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-8	25°C		-42		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-9	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-9	25°C		-42		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Figure 7-10	25°C		65		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		13		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		76		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		85		pF

(1) When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

6.6 Electrical Characteristics (VDD = 3.3 V ±10 %)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		9		Ω
			–40°C to +85°C			15	Ω
			–40°C to +125°C			17	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		0.15		Ω
			–40°C to +85°C			1	Ω
			–40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		3		Ω
			–40°C to +85°C		5		Ω
			–40°C to +125°C		6		Ω
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Figure 7-2	25°C		±75		nA
			–40°C to +85°C	-150		150	nA
			–40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Figure 7-2	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to Figure 7-3	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Input logic high		-40°C to 125°C	1.35		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.10	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.01		µA
			–40°C to +125°C			1.5	µA

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-4	25°C		14		ns
			–40°C to +85°C			25	ns
			–40°C to +125°C			25	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-5	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		17		ns
			–40°C to +85°C			25	ns
			–40°C to +125°C			25	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		7		ns
			–40°C to +85°C			13	ns
			–40°C to +125°C			13	ns
Q_C	Charge Injection	$V_S = V_{DD}/2$ R_S = 0 Ω, C_L = 1 nF Refer to Figure 7-7	25°C		±7		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-8	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-8	25°C		-42		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-9	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-9	25°C		-42		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Figure 7-10	25°C		65		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		13		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		76		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		85		pF

(1) When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

6.7 Electrical Characteristics (VDD = 1.8 V ±10 %)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		0.15		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 1.98 V Switch Off V_D = 1.8 V / 1 V V_S = 1 V / 1.8 V Refer to Figure 7-2	25°C		±75		nA
			–40°C to +85°C	-150		150	nA
			–40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 1.98 V Switch Off V_D = 1.8 V / 1 V V_S = 1 V / 1.8 V Refer to Figure 7-2	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.8 V / 1 V Refer to Figure 7-3	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.10	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.006		µA
			–40°C to +125°C			0.95	µA

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-4	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-5	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		28		ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		16		ns
			–40°C to +85°C			27	ns
			–40°C to +125°C			27	ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF Refer to Figure 7-7	25°C		-2		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-8	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-8	25°C		-42		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-9	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-9	25°C		-42		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Figure 7-10	25°C		65		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		13		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		76		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		85		pF

(1) When V_S is 1.8 V, V_D is 1 V or when V_S is 1 V, V_D is 1.8 V.

6.8 Electrical Characteristics (VDD = 1.2 V ±10 %)

at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to Figure 7-1	25°C		0.15		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1.2 V / 1 V V_S = 1 V / 1.2 V Refer to Figure 7-2	25°C		±75		nA
			–40°C to +85°C	-150		150	nA
			–40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1.2 V / 1 V V_S = 1 V / 1.2 V Refer to Figure 7-2	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1.2 V / 1 V Refer to Figure 7-3	25°C		±200		nA
			–40°C to +85°C	-500		500	nA
			–40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.10	µA
C_{IN}	Logic input capacitance		25°C		1		pF
			–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.005		µA
			–40°C to +125°C			0.8	µA

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-4	25°C		60		ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			210	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-5	25°C		32		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{ON(EN)}$	Enable turn-on time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		60		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
$t_{OFF(EN)}$	Enable turn-off time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF Refer to Figure 7-6	25°C		45		ns
			–40°C to +85°C			150	ns
			–40°C to +125°C			150	ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF Refer to Figure 7-7	25°C		-2		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-8	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-8	25°C		-42		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Figure 7-9	25°C		-62		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Figure 7-9	25°C		-42		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Figure 7-10	25°C		65		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		13		pF
C_{DOFF}	Drain off capacitance	f = 1 MHz	25°C		76		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		85		pF

(1) When V_S is 1.2 V, V_D is 1 V or when V_S is 1 V, V_D is 1.2 V.

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown below. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed as shown in Figure 7-1 with $R_{ON} = V / I_{SD}$:

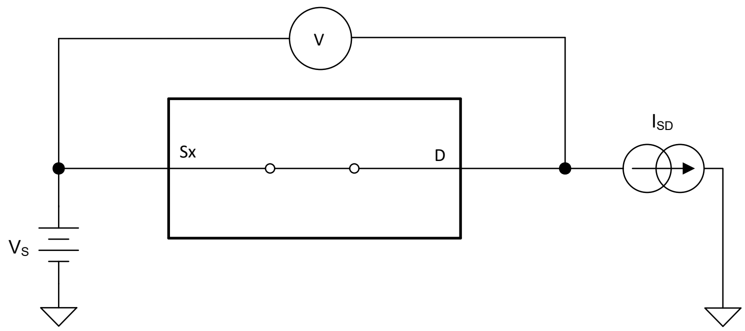


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 7-2.

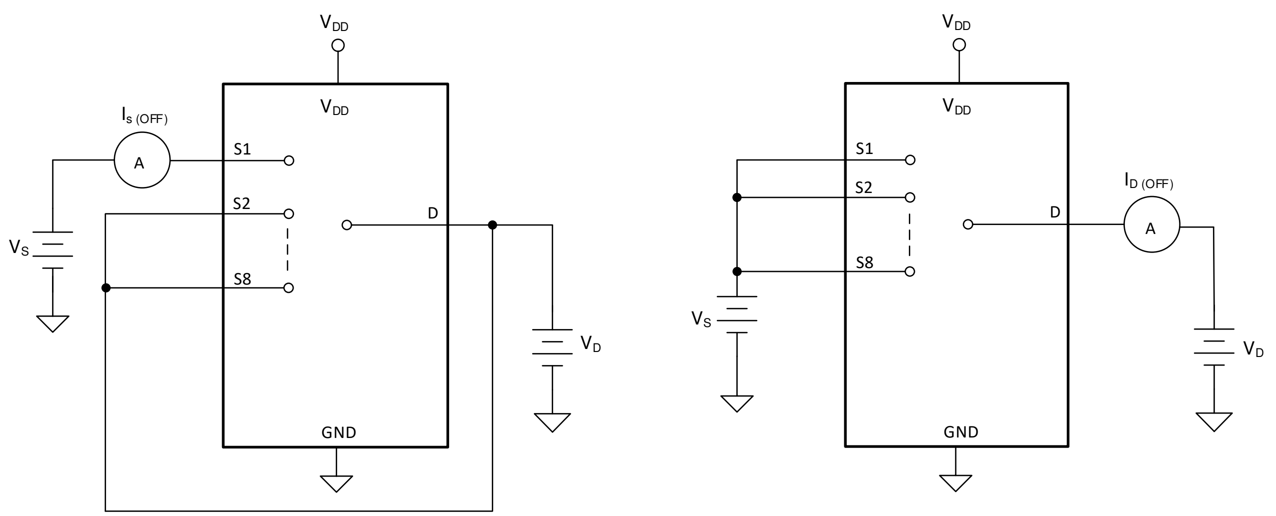


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

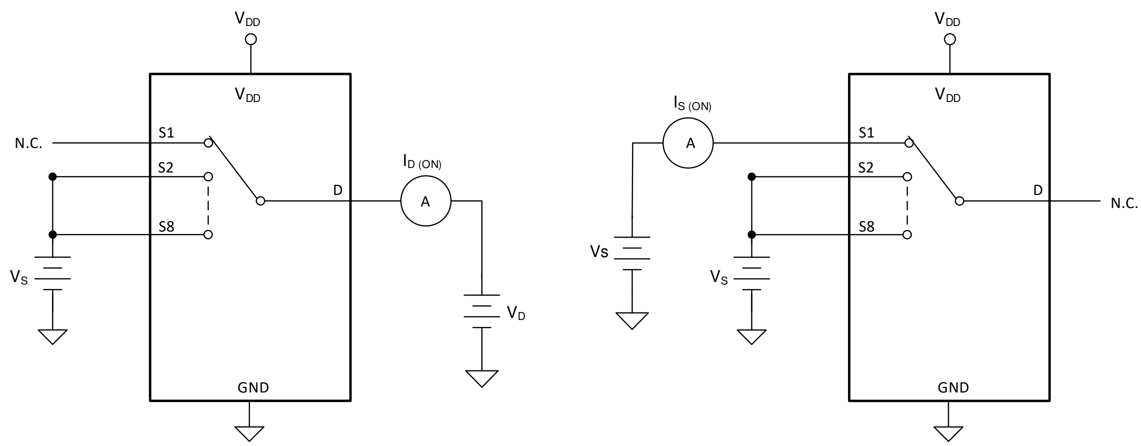


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

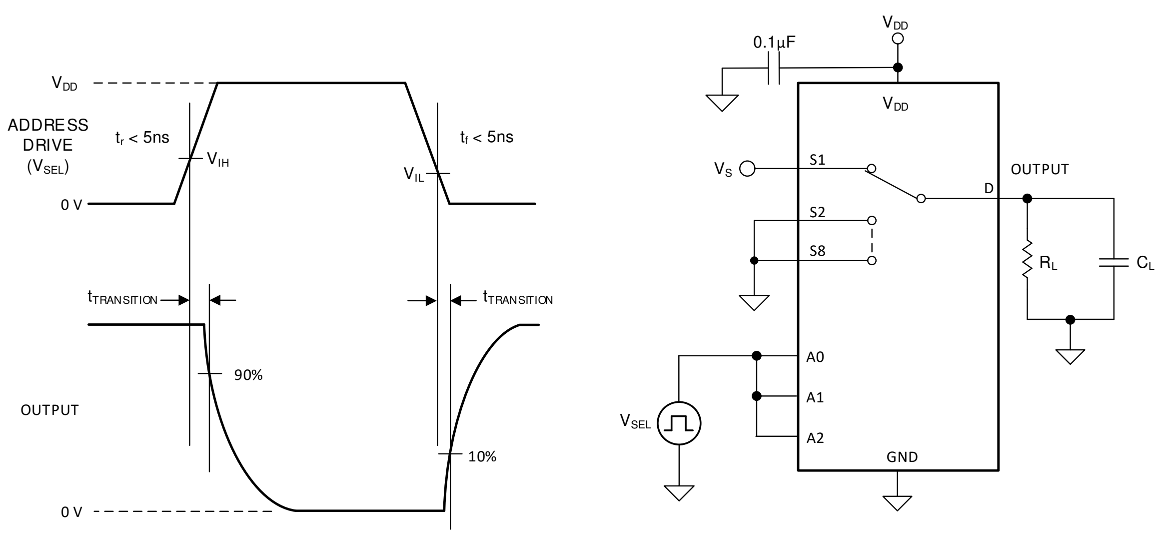


Figure 7-4. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

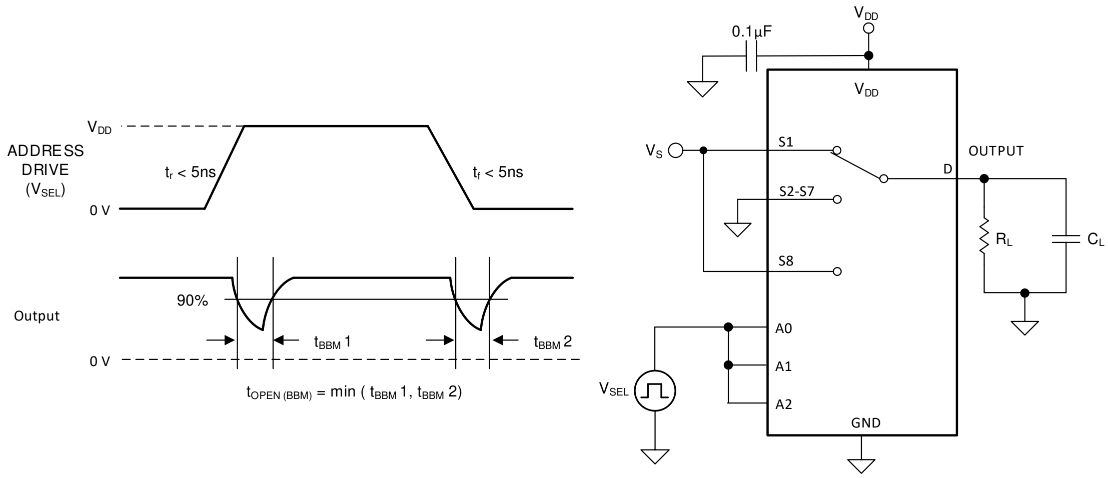


Figure 7-5. Break-Before-Make Delay Measurement Setup

7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device, system level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-6 shows the setup used to measure transition time, denoted by the symbol $t_{OFF(EN)}$.

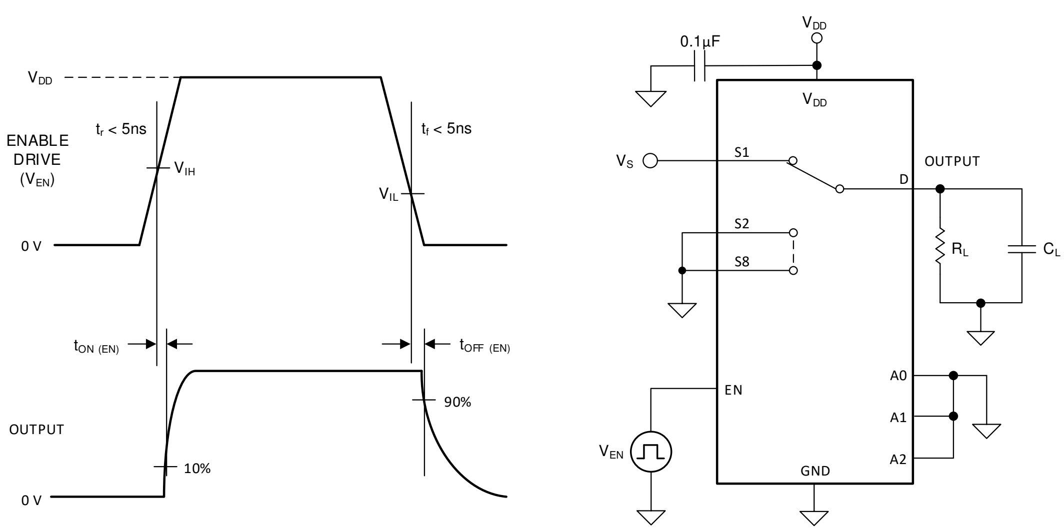


Figure 7-6. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUX1208-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 7-7 shows the setup used to measure charge injection from source (Sx) to drain (D).

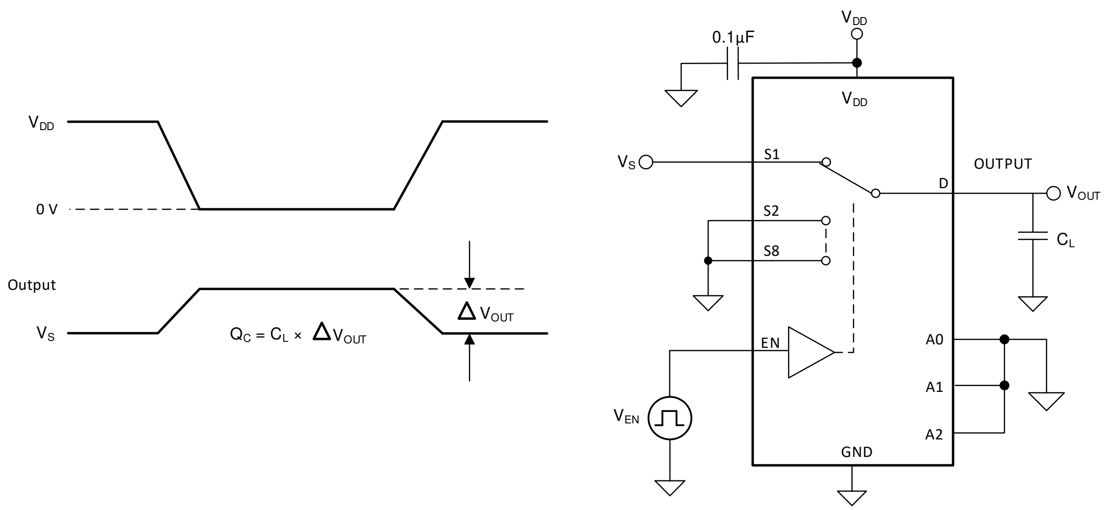


Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-8 shows the setup used to measure, and the equation to compute off isolation.

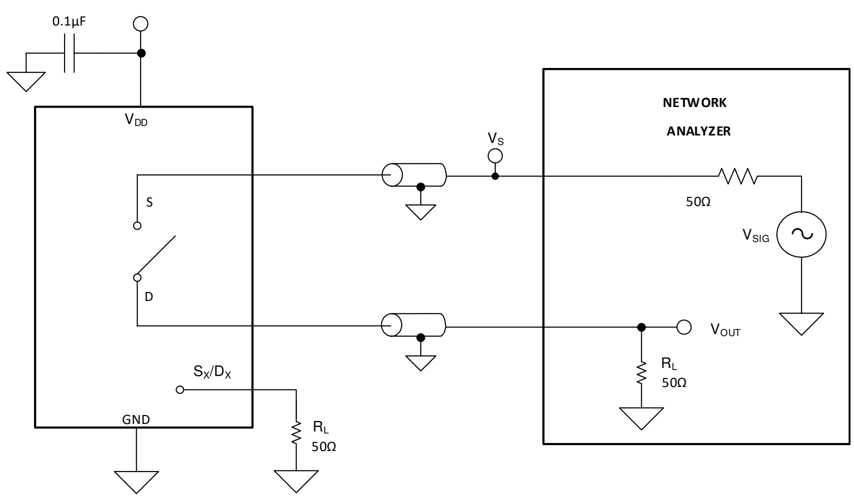


Figure 7-8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{1}$$

7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 7-9 shows the setup used to measure, and the equation used to compute crosstalk.

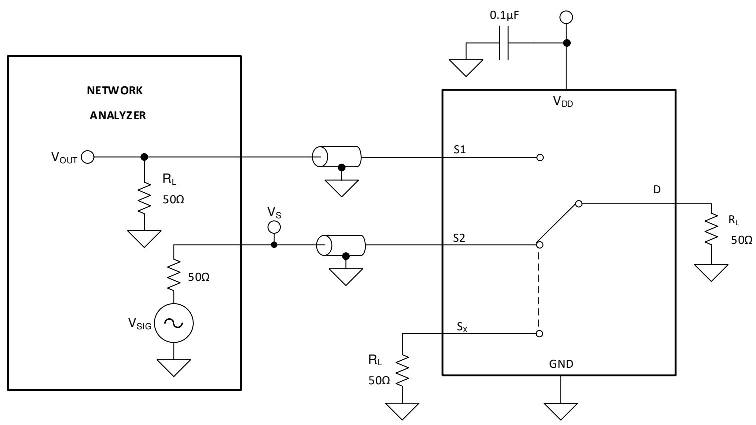


Figure 7-9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 7-10 shows the setup used to measure bandwidth.

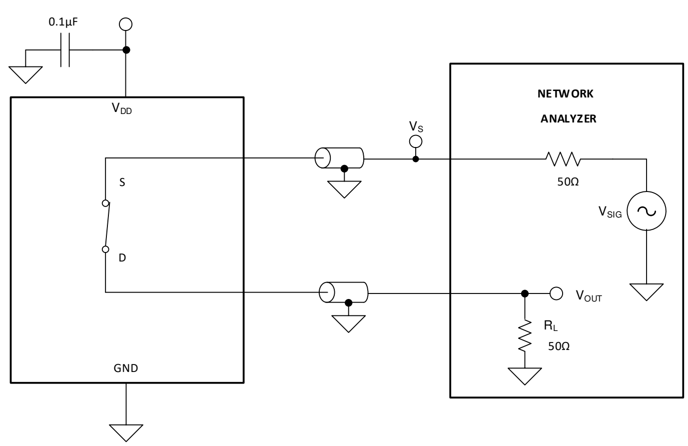


Figure 7-10. Bandwidth Measurement Setup

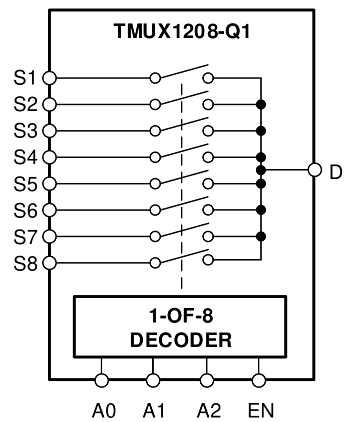
$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{3}$$

8 Detailed Description

8.1 Overview

The TMUX1208-Q1 is an 8:1, single-ended (1-channel), mux. Each channel is turned on or off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX1208-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1208-Q1 ranges from GND to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

The TMUX1208-Q1 has 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the multiplexers to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

8.3.4 Fail-Safe Logic

The TMUX1208-Q1 has Fail-Safe Logic on the control input pins (EN, A0. A1, A2) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1208-Q1 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the multiplexers with V_{DD} = 1.2 V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

8.3.5 Device Functional Modes

When the EN pin of the TMUX1208-Q1 is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state regardless of the state of the address lines.

The TMUX1208-Q1 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or D) should be connected to GND.

8.3.6 Truth Tables

Table 8-1 shows the truth tables for the TMUX1208-Q1.

Table 8-1. TMUX1208-Q1 Truth Table

EN	A2	A1	A0	Selected Inputs Connected To Drain (D) Pin
0	X(1)	X(1)	X(1)	All channels are off
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denotes *don't care*.

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08 V to 5.5 V). These devices include 1.8 V logic compatible control input pins that enable operation in systems with 1.8 V I/O rails. Additionally, the control input pins support Fail-Safe Logic which allows for operation up to 5.5 V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features make the TMUX12xx a family of general purpose multiplexers and switches that can reduce system complexity, board size, and overall system cost.

9.2 Typical Application

One useful application to take advantage of the TMUX1208-Q1 features is multiplexing various signals into an ADC that is integrated into a MCU. Using an integrated ADC in a MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs/sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/O.

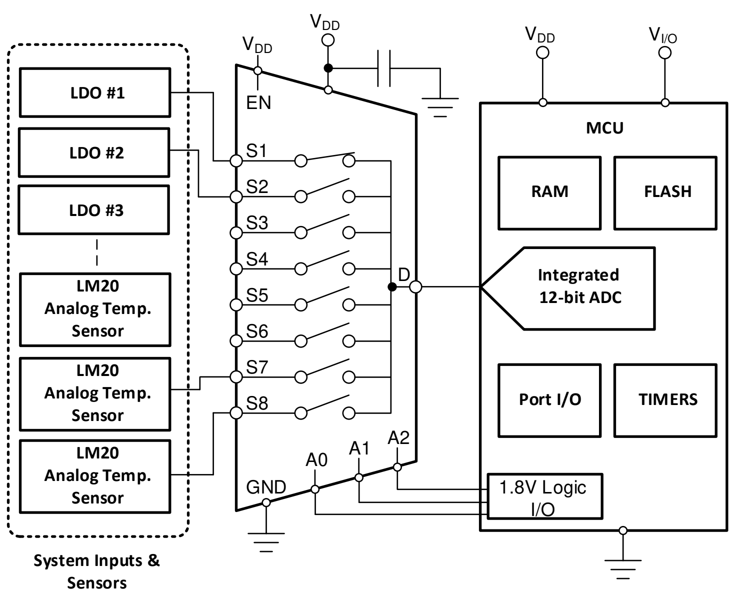


Figure 9-1. Multiplexing Signals to Integrated ADC

9.3 Design Requirements

For this design example, use the parameters listed in Table 9-1.

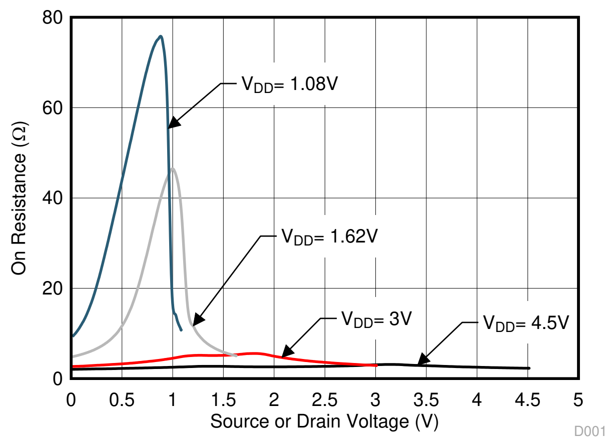
Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5.0 V
I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible

9.4 Detailed Design Procedure

The TMUX1208-Q1 can be operated without any external components except for the supply decoupling capacitors. If the parts desired power-up state is disabled, the enable pin should have a weak pull-down resistor and be controlled by the MCU via GPIO. All inputs being muxed to the ADC of the MCU must fall within the recommend operating conditions of the TMUX1208-Q1 including signal range and continuous current. For this design with a supply of 5 V, the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

9.5 Application Curve



T_A = 25°C

Figure 9-2. On-Resistance vs Source or Drain Voltage

9 Power Supply Recommendations

The TMUX1208-Q1 operate across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

10 Layout

10.1 Layout Guidelines

10.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

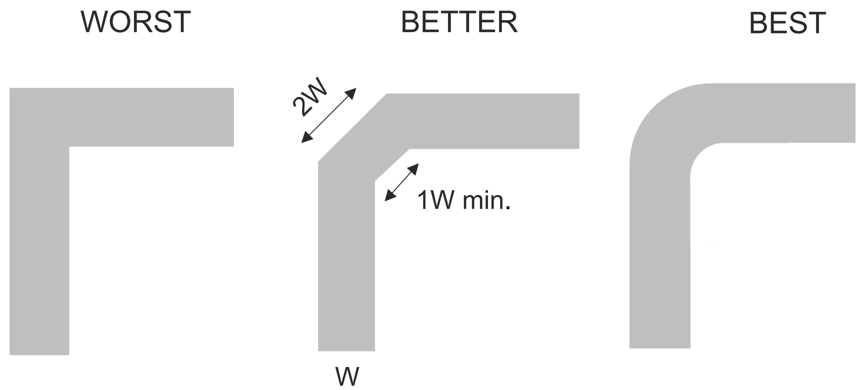


Figure 10-1. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

10.1.2

Figure 10-2 illustrates an example of a PCB layout with the TMUX1208-Q1. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example

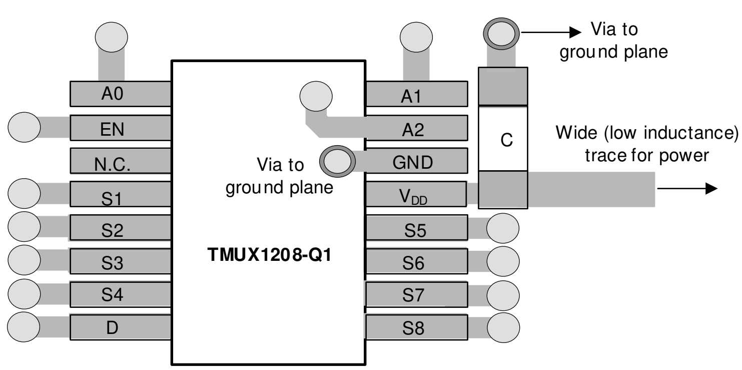


Figure 10-2. TMUX1208-Q1 Layout Example

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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12 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1208QRSVRQ1	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	208Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMUX1208-Q1 :

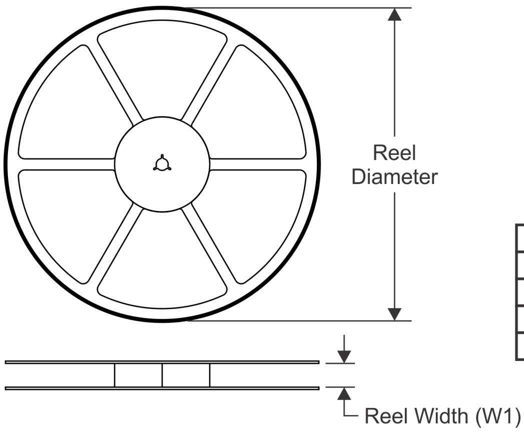
- Catalog: TMUX1208

NOTE: Qualified Version Definitions:

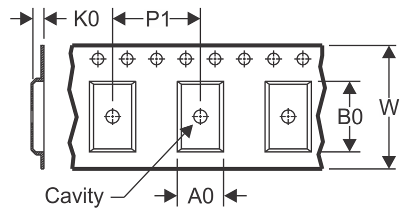
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

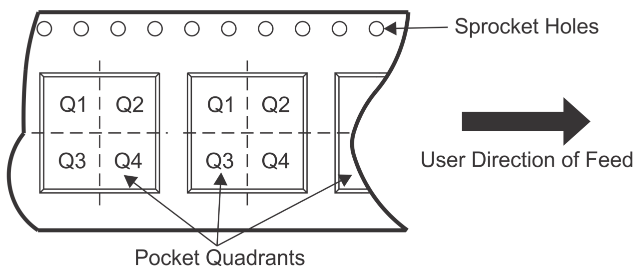


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

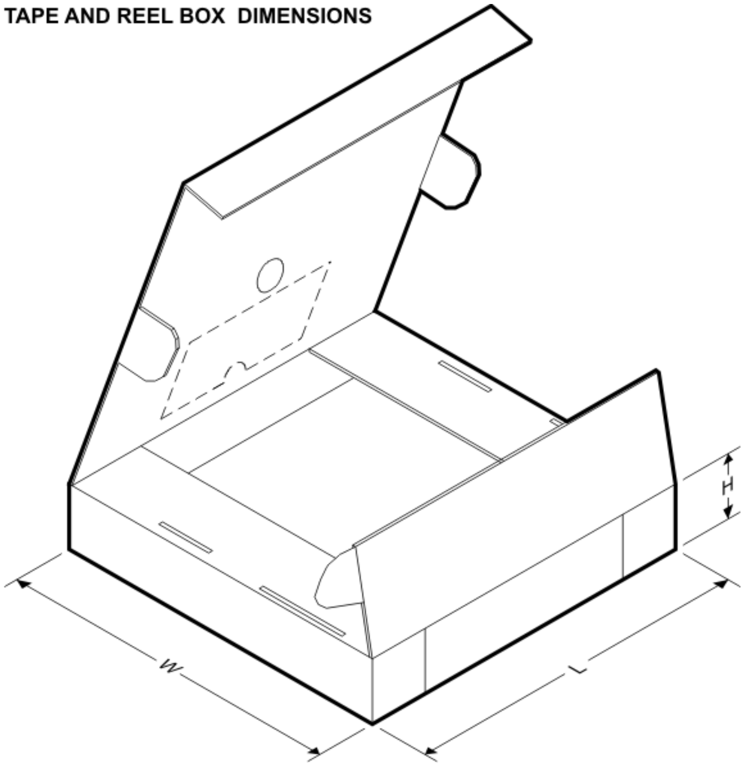
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

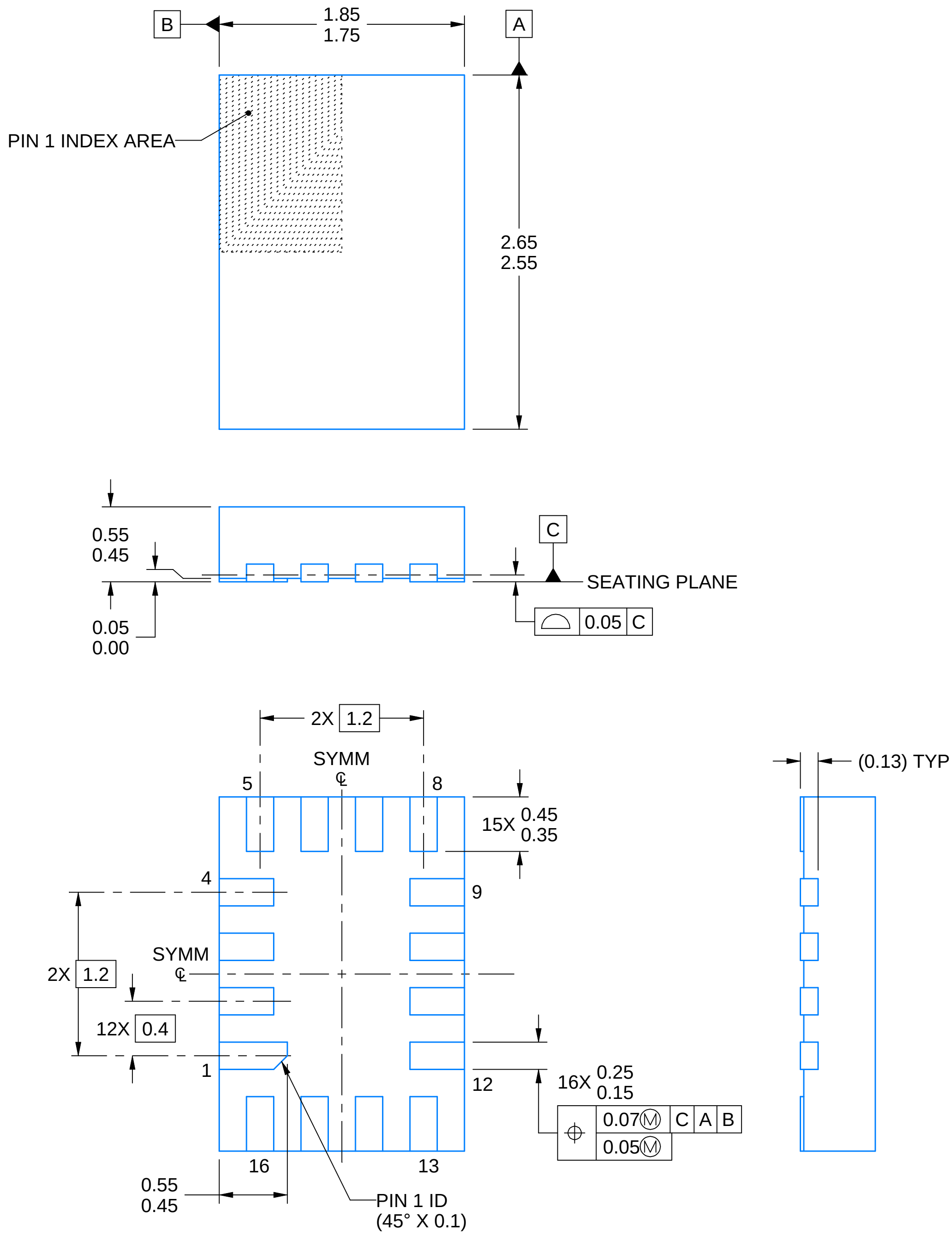
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1208QRSVRQ1	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1208QRSVRQ1	UQFN	RSV	16	3000	189.0	185.0	36.0



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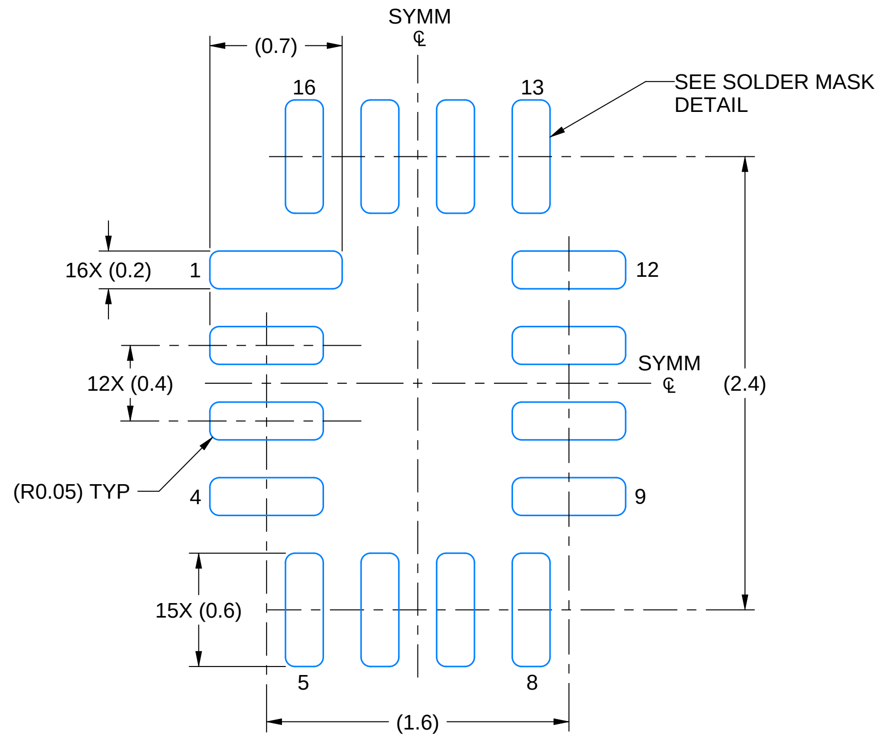
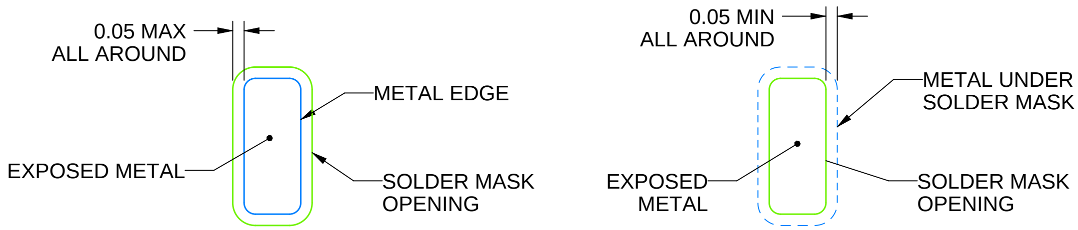
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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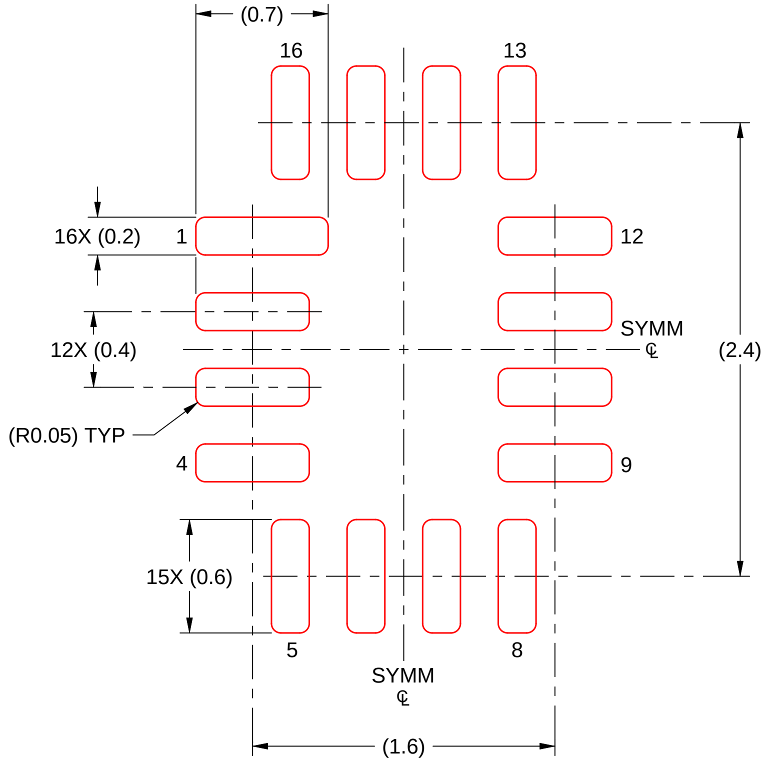
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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